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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,408	01/08/2002	Naoki Fukutomi	7426-082	9036
20457	7590	03/07/2006	EXAMINER	
ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-3873			DOTY, HEATHER ANNE	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,408	FUKUTOMI ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 32,35-37 and 41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 32,35-37 and 41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 July 2003 and 28 August 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 08/716,362.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>7/12/05, 8/18/05</u> | 6) <input checked="" type="checkbox"/> Other: <u>IDS 1/17/06</u> |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/17/2006 has been entered.

Claim Objections

Claim 32 is objected to because of the following informalities: in line 19, "semiconductcor" should be changed to "semiconductor." Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 32, 36, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ackermann et al. (U.S. 4,975,765) in view of Yamaguchi (U.S. 5,250,470).

Regarding claim 32, Ackermann et al. teaches a substrate for semiconductor packages having an insulating supporting member (17 in Fig. 3) and plural sets of

wirings (19 and 20 in Fig. 3B) formed on one side of said insulating supporting member, and further comprising a semiconductor device mounting region (2 in Fig. 3A, 3B) and a resin-sealing semiconductor package region (11 in Fig. 3E) outside of said semiconductor device mounting region, wherein said wirings comprise a predetermined wiring pattern (20 in Fig. 3B) including wire-bonding terminals (19 in Fig. 3) and external connection terminals (ends of lines 20 in Fig. 3B), wherein said wire-bonding terminals are provided in said semiconductor package region and said external connection terminals are provided only within said semiconductor device mounting region (Fig. 3B), and wherein openings (18 in Fig. 3C) are provided in said insulating supporting member at points where said external connection terminals are formed, reaching said external connection terminals.

Ackermann et al. does not disclose that plural sets of said semiconductor device mounting region and said semiconductor package region are formed on said insulating supporting member, wherein said plurality of said semiconductor device mounting regions and semiconductor package regions have blocks of said wirings, each having a same wiring pattern.

Yamaguchi teaches a method of forming plural sets of sets of identical blocks of wiring on a substrate for semiconductor packages (Fig. 10). This method allows for multiple chips to be manufactured together on a single substrate, and subsequently separated (column 5, lines 17-19).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to make the substrate with the wiring pattern and semiconductor

package region taught by Ackermann et al., and repeat this structure a plurality of times on a single substrate, as taught by Yamaguchi. The motivation for doing so at the time of the invention would have been to increase device production by manufacturing multiple semiconductor packages on a single substrate and subsequently separating them, as taught by Yamaguchi.

Regarding claim 36, Ackermann et al. and Yamaguchi together teach the substrate of claim 32. Ackermann et al. further teaches that the external connection terminals are arranged in a grid pattern at positions corresponding to a semiconductor device mounting region of said substrate (Fig. 3B).

Regarding claim 41, Ackermann et al. and Yamaguchi together teach the substrate according to claim 32. Ackermann et al. teaches that the sets of wirings can be formed on both sides of the substrate (implying that they can also be formed on only one side), but Yamaguchi teaches forming sets of wiring only on one side of the insulating supporting member.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form the wirings on only side of the insulating supporting member, as taught by Yamaguchi, since Yamaguchi teaches that it is known in the art to form wiring on only one side of the substrate surface, and forming the wiring on both sides would increase the number of processing steps involved in manufacturing the packaging.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ackermann et al. (U.S. 4,975,765) in view of Yamaguchi (U.S. 5,250,470), as applied to claim 32 above, and further in view of Enomoto et al. (U.S. 5,175,060).

Ackermann et al. and Yamaguchi together teach the substrate of claim 32 (note 35 U.S.C. 103(a) rejection above). Ackermann et al. further discloses chemically depositing a nickel and gold layer on the wire-bonding terminal (column 5, lines 49-53), but does not expressly disclose a gold plate layer.

Enomoto et al. teaches that it is advantageous to plate a wire-bonding surface with nickel and gold to enhance the connection reliability of the wire to be bonded (column 6, lines 16-25).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to make the substrate taught by Ackermann et al. and Yamaguchi together, and further add a nickel layer and gold plate layer to the wire-bonding terminal, as taught by Enomoto et al. to be advantageous for enhancing the connection reliability of the wire to the bonding surface.

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ackermann et al. (U.S. 4,975,765) in view of Yamaguchi (U.S. 5,250,470), as applied to claim 32 above, and further in view of Lombard et al. (U.S. 4,890,383) and Pennisi et al. (U.S. 5,313,365).

Regarding claim 37, Ackermann et al. and Yamaguchi together teach a semiconductor package produced by a method comprising the steps of mounting a semiconductor device on each of said plural semiconductor device mounting regions of

the substrate for semiconductor packages according to claim 32 (note 35 U.S.C. 103(a) rejection above). Ackermann et al. further teaches electrically connecting the semiconductor devices with the wire-bonding terminals by wire bonding (column 5, lines 59-63) and sealing said semiconductor package region including said semiconductor device with a sealing resin connected in one piece (column 6, lines 3-18). Yamaguchi further teaches employing a die-bonding material to mount a semiconductor device on each of said plural semiconductor device mounting regions of the substrate (column 5, lines 1-6), and cutting said substrate for semiconductor packages to be separated into the individual semiconductor packages (column 5, lines 17-19).

Ackermann et al. teaches forming bumps on said external connection terminals (21 in Figs. 3 and 5), but does not teach that they are solder bumps. Additionally, neither Ackermann nor Yamaguchi teaches cutting the substrate and the sealing resin in one operation.

Lumbard et al. teaches mounting a plurality of semiconductor chips on a substrate, encapsulating the chips and associated wiring in a sealing resin, and cutting the substrate and the sealing resin in one operation to be separated into the individual semiconductor package (column 2, lines 1-37). Lumbard et al. teaches that this method is suitable for fully automated, and therefore low-cost, production.

Pennisi et al. teaches forming solder bumps on the underside of a packaging substrate connected to a semiconductor die via plated through holes.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to make the substrate taught by Ackermann et al. and Yamaguchi together, and further use a die-bonding material to mount a semiconductor device on each of said plural device mounting regions of the substrate, as taught by Yamaguchi, to facilitate fixing the die to the mounting area.

Also at the time of the invention, it would have been obvious to one of ordinary skill in the art to make the substrate taught by Ackermann et al. and Yamaguchi together, and further cut the substrate and sealing resin in one operation to be separated into the individual semiconductor package, as taught by Lumbard et al. to be part of a fully automated and low-cost production.

Also at the time of the invention, it would have been obvious to one of ordinary skill in the art to use solder bumps on the external connection terminals, since Ackermann et al. teaches using bumps on the external connection terminals, and Pennisi et al. further teaches that solder bumps specifically are appropriate in such an arrangement of device and packaging features.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

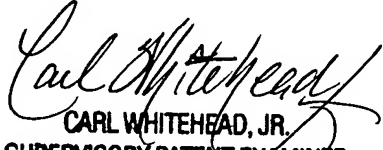
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had


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